In the Claims:

Please amend the claims as follows:

1. (Previously Presented) A computer system, comprising:

multiple processors;

a plurality of resources assigned to node groups;

a first descriptor of respective topological levels of at least one of the resources, said first descriptor including an extended system descriptor;

said first descriptor having a pointer to a second descriptor of said resources, said second descriptor including a node descriptor referenced in said first descriptor;

said second descriptor including a node identifying number that identifies a path of interconnectivity of a resource in system topology, and a node number that identifies a node within said topology, said node identifying number and said node number being separate identifiers;

wherein the first and second descriptors are produced by a same firmware in a single computer system and said firmware is maintained as a data structure.

2. (Previously Presented) The system of claim 1, wherein said first descriptor is a first level data structure, and said second descriptor is a primary data structure.

3. (Original) The system of claim 2, wherein said primary data structure comprises a pointer to a secondary data structure.

4. (Previously Presented) The system of claim 1, wherein said firmware stores topology information of system resources in a data structure.

5. (Previously Presented) The system of claim 1, wherein said node identifying number is a

string of multiple octets with a value stored in each octet identifying a location of a node.

6. (Original) The system of claim 1, further comprising a dynamic updator of at least the first and second descriptors.

7. (Original) The system of claim 6, wherein said dynamic updator reflects real-time system configuration into the first descriptor.

8. (Original) The system of claim 6, wherein said dynamic updator reflects real-time system performance into the second descriptor.

9. (Previously Presented) The system of claim 1, wherein said second descriptor includes a pointer to a secondary data structure having a descriptor selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors, and share cache descriptors.

10. (Previously Presented) The system of claim 9, wherein said shared cache descriptor reflects interconnects of the system.

11. (Original) The system of claim 10, wherein said shared cache descriptor reflects latencies of the interconnects.

12. (Previously Presented) The system of claim 1, wherein said second descriptor reflects average latency between the node groups.

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